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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,178	09/30/2003	Shahrokh Shahidzadeh	884.912US1	6782

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EXAMINER	
TANG, SON M	

ART UNIT	PAPER NUMBER
2632	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,178	SHAHIDZADEH ET AL.	
	Examiner	Art Unit	
	Son M. Tang	2632	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/14/05, (Amendment)*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **4, 11 and 17-29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori et al. [US 6,891,214; Mori] in view of Perner [US 6,694,282].

Regarding claims 17-18, 20 and 21-22: Mori discloses an apparatus comprising: -a memory (8) to store a selected number of out-of-specification (over-current) input operational conditions encountered by an electronic circuit (1), that met by recording an over-current detection in a non-volatile memory (8); and determining a specified number of recorded over-current conditions and display at display unit 911 [see Fig. 12 and 9, col. 3, lines 54-66, col. 4, lines 48-58 and col. 10 lines 30-35], wherein the input operational is the power input from the power source to a semiconductor through current sensor IGBT (4) [see Fig. 1 and col. 3, lines 4-25], Mori stores out-of-specification number in a non-volatile memory, but lacks of specifically that said non-volatile memory is an indelible memory. Perner teaches a semiconductor component comprises a PROM memory (unchangeable data memory includes a fuse map) to store the temperature measurement [see col. 2, lines 50-67], wherein PROM memory (program read only memory) it is a one type of indelible memory. Therefore, it would have been obvious of one having ordinary skill in the art to use PROM memory to store information as taught by Perner, so the information can be protected from damage or erased.

Regarding claim 19: Mori and Perner disclose all the limitations as described above, except that not specific about a filter module coupled to the detection module (721), it is known that in order to determine an over-current condition, the current measured signal has to be filtered the noise signal for a pure detected signal, therefore, it would have been is obvious of one having ordinary skill in the art that the system has a filter module to filter out noise signal for purpose of accuracy.

Regarding claims 23 and 28: Mori and Perner disclose all the limitations as described above, Mori further discloses that the electronic circuit comprises a microprocessor (3, 730, 720, 710, 700) [see Fig. 1].

Regarding claim 24-25: Mori and Perner disclose all the limitations as described above, except for not specifically teaches a logic module that comprises an analog-to digital converter. Since, the measurement signal is in analog, in order to store in memory the analog signal must converted to digital, therefore, it would have been obvious to one having ordinary skill in the art that the logic module comprises an analog-to-digital converter should be included in the system for performing the converting signal.

Regarding claims 26-27: Mori and Perner disclose all the limitations as described above, Mori further teaches a recommended operations specified condition upper limit (predetermined current flows) associated with an integrated circuit they are not specifically teach a memory to store a specified condition to be compared with an operational

Regarding claim 29: Mori and Perner disclose all the limitations as described above, Mori further discloses a basic input-output system (9) [see Fig. 1].

Regarding claims 4 and 11: The claimed method steps are interpreted and rejected as rejection stated above.

3. Claims **1-3, 5-10, 12-15, 17, 21 and 26-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori et al. [US 6,891,214; Mori] in view of Goodfellow et al. [US 2004/0150928; Goodfellow] and further in view of Perner [US 6,694,282].

Regarding claims 12, 14 and 17: Mori discloses an article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing:

-comparing an input operational current with a specified current and recording an over-current detections in a non-volatile memory (8); and determining a specified number of recorded input over-current conditions and display at display unit 911 [see Fig. 12 and 9, col. 3, lines 54-66, col. 4, lines 48-58 and col. 10 lines 30-35], wherein the input operational is the power input from the power source to a semiconductor through current sensor IGBT (4) [see Fig. 1 and col. 3, lines 4-25], Mori stores the IC failure histories (current and temperature) and display the number of failure times, but does not specifically disclose an over-voltage condition, Goodfellow teaches a system which comprises a fault conditions monitoring of the ICs (102-106) including over-voltage conditions [see ¶ 0032]. It would have been obvious of one having ordinary skill in the art at the time of the claimed invention, to have a voltage monitor as taught by Goodfellow in the IC failure histories monitor of Mori, in order to provide additional information about the IC operation history.

Mori uses non-volatile memory for storing failure history, but lacks of specifically disclose that non-volatile memory is an indelible memory. Perner teaches a semiconductor component comprises a PROM memory (unchangeable data memory includes a fuse map) to store the temperature measurement [see col. 2, lines 50-67], wherein PROM memory (program read only memory) it is a one type of indelible memory. Therefore, it would have been obvious of one having ordinary skill in the art to use PROM memory to store information as taught by Perner, so the information can be protected from damage or erased.

Regarding claim 13: Mori, Goodfellow and Perner disclose all the limitations as described above, except that not specific about filtering the operational voltage for at least a duration of one clock period. In order to determine over-voltage, the measured signal during a duration of one clock period has to be filtered and get rid of noise signal, therefore, it would have been is obvious of one having ordinary skill in the art to recognize that the detected signal has to be filtered at least one clock period to get a pure detected signal for the purpose of better accuracy.

Regarding claim 15: Mori, Goodfellow and Perner disclose all the limitations as described above, except for not specifically teach that the specified voltage selected amount is at least about two times greater than an expected noise voltage value. In order to have an accuracy detected signal, the threshold value has to be higher than the noise value, therefore, it is obvious to one having ordinary skill in the art that any appropriate value higher than noise voltage value can be implement, including two times greater than an expected noise voltage value as claimed.

Regarding claim 21: Mori and Perner disclose all the limitations as described above, except for not specifically disclose an over-voltage condition, Goodfellow teaches a

system which comprises a fault conditions monitoring of the ICs (102-106) including an over-voltage condition [see ¶ 0032]. It would have been obvious of one having ordinary skill in the art at the time of the claimed invention, to have a voltage monitor as taught by Goodfellow in the IC failure histories monitor of Mori, in order to provide additional information about the voltage condition in an IC operation history.

Regarding claims 26-27: Mori and Perner disclose all the limitations as described above, Mori further teaches a recommended operations specified condition upper limit (predetermined current flows) associated with an integrated circuit [col. 7, lines 55-65], and the predetermined condition should be stored in a memory that inherently included in the system. Mori and Perner fail to specify that the specified condition is a voltage. Goodfellow teaches a system which comprises a fault conditions monitoring of the ICs (102-106) including an over-voltage condition [see ¶ 0032]. It would have been obvious of one having ordinary skill in the art at the time of the claimed invention, to have a voltage monitor as taught by Goodfellow in the IC failure histories monitor of Mori, in order to provide additional information about the voltage condition in an IC operation history.

Regarding claims 1-3, 5-10: The claimed method steps are interpreted and rejected as rejection stated above.

Response to Arguments

4. Applicant's arguments with respect to claims 1, 4-6, 8-9, 11-14, 16-18, 21-22, 24, 27-29 have been considered but are moot in view of the new ground(s) of rejection.

5. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the

teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, any type of out-of- specification detection such as over-current, over-voltage or over-temperature would cause damage to the semiconductor. Therefore, it would have been made it obvious that over-voltage monitor is analogous to any other types, which would equally affect the semiconductor.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son M. Tang whose telephone number is (571)272-2962. The examiner can normally be reached on 4/9 First Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Daniel J. Wu can be reached on (571)272-2964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Son Tang

Thomas J. Mullen, Jr.
Primary Examiner
Art Unit 2632

1-23-06